



# Reliable GPS position on an unreliable hardware

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## OBJECTIVES

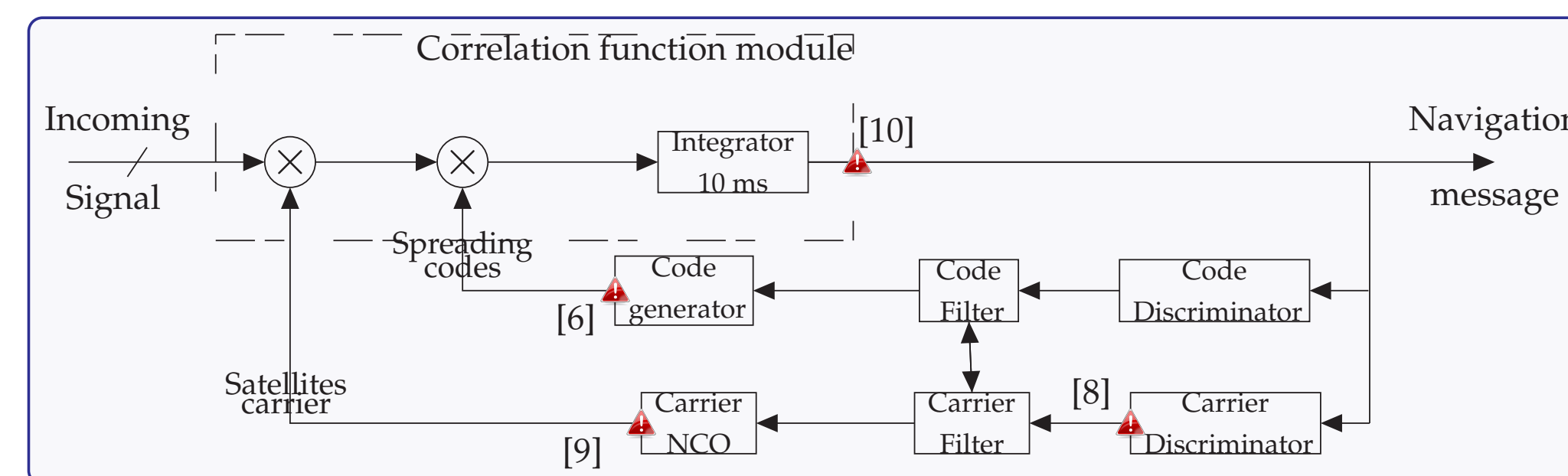
This work address the **fault tolerance** topic in the **GPS context**. Starting from a **noiseless GPS receiver**, redundant mechanisms can be added to design a more resilient GPS receiver in the presence of errors due to process, voltage and temperature (PVT) variations [1]. These mechanisms are based on different layer of abstraction to guarantee a mutual trade-off of **system performance** (quality of the position given by the GPS receiver), **hardware reliability** and **implementation complexity**. An Application-specific integrated circuit (**ASIC**) will be designed with two versions of the GPS receiver: the **standard** version, and a **complex** version where fault tolerant techniques are added to make the GPS receiver **more tolerant to errors**.

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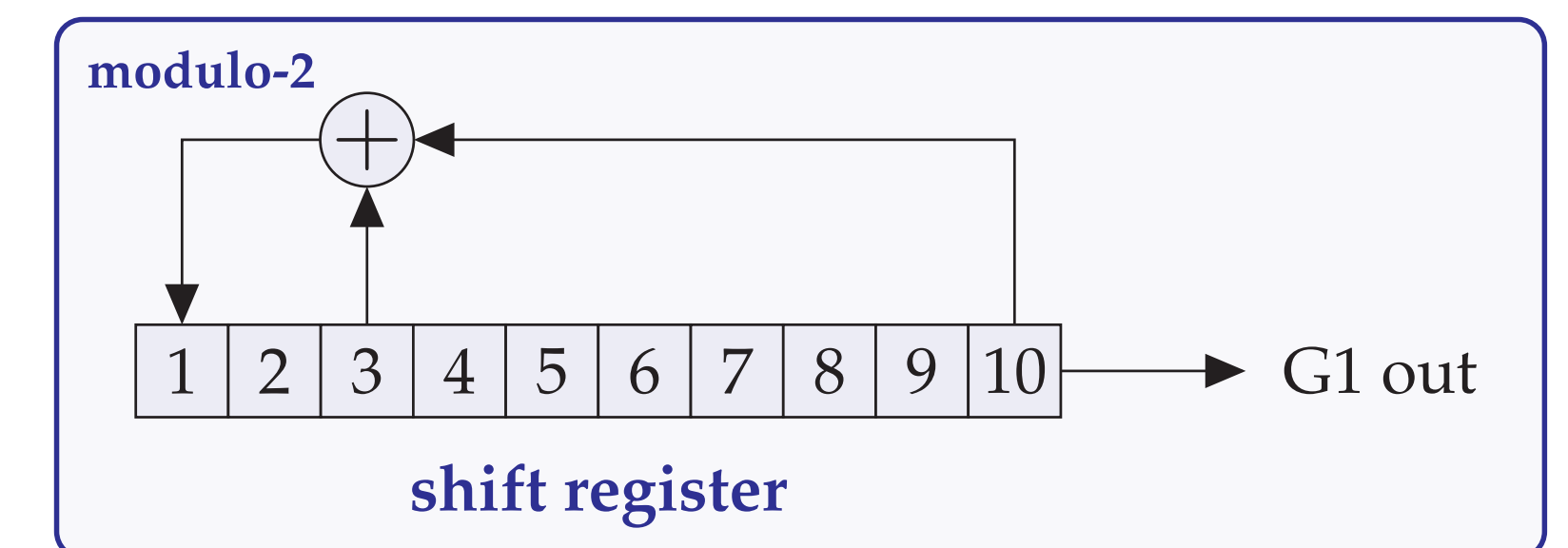
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## INTRODUCTION

- There is continual motivation to **reduce power consumption** and **extend battery life** of mobile devices.
- Power consumption and device lifetime can be improved by operating at **minimal supply voltage**, which increases the likelihood of **momentary/persistent faults**.
- GPS satellite signals are made of three components: **spreading code**, **carrier** and **navigation message**.
- Tracking GPS satellite signals evolves three main process:
  - **GPS receivers** use, **Numerically controlled oscillators** (NCO), to produce a local copy of the carrier of incoming satellite signals. Moreover, copies of spreading codes of GPS satellites are produced, locally, by two 10-stage LFSR (Linear feedback shift register) modules, designated G1 and G2.
  - A **correlation function** is computed every 10 ms between local signals and incoming signals. A **maximum correlation output** is achieved when the two signals are time **aligned**.
  - Two **feedback loops** are used to update the local generated signals over time, since satellites are in continuous motion and the receiver is also dynamic. Each loop is made of **discriminators** and **filters**.

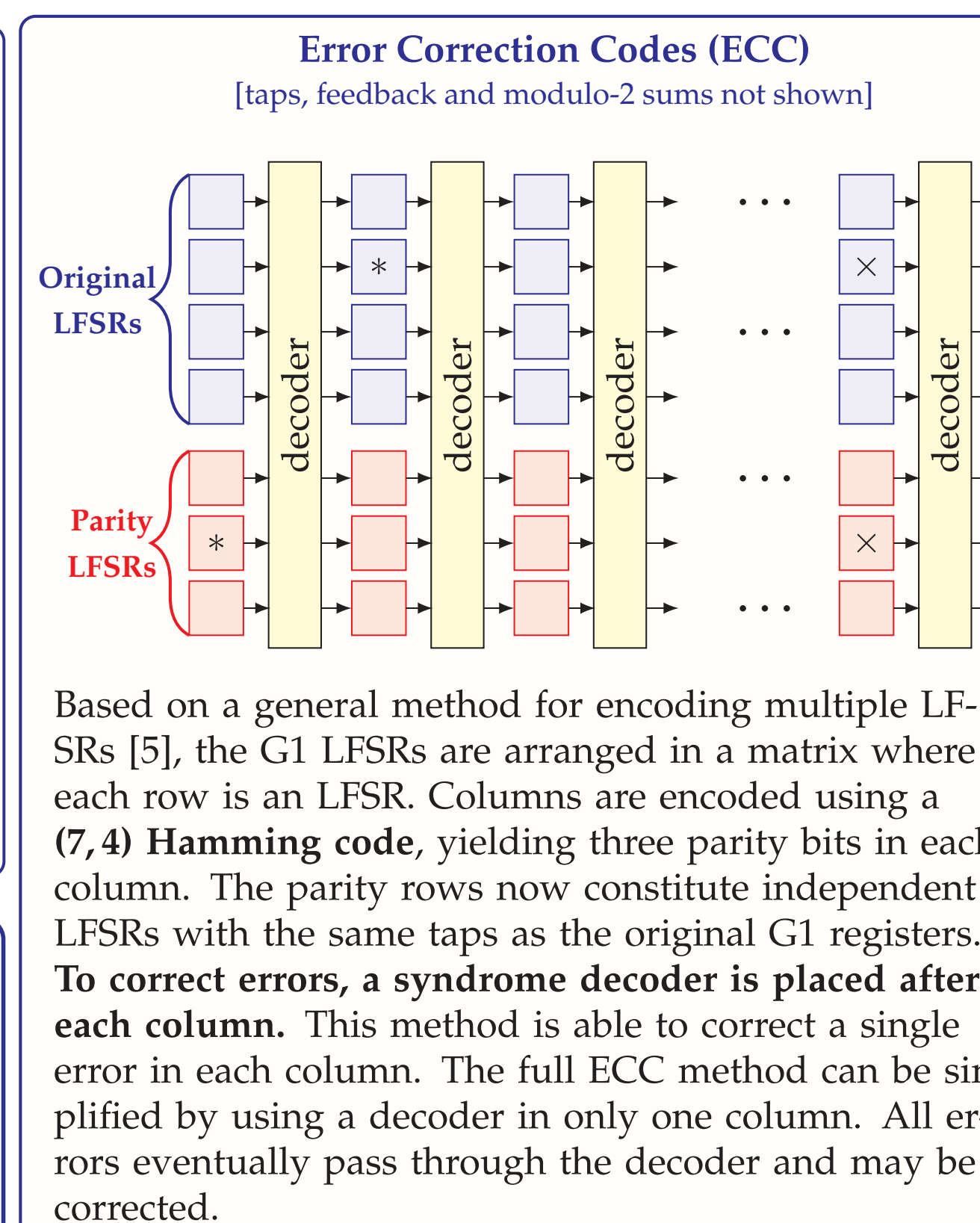
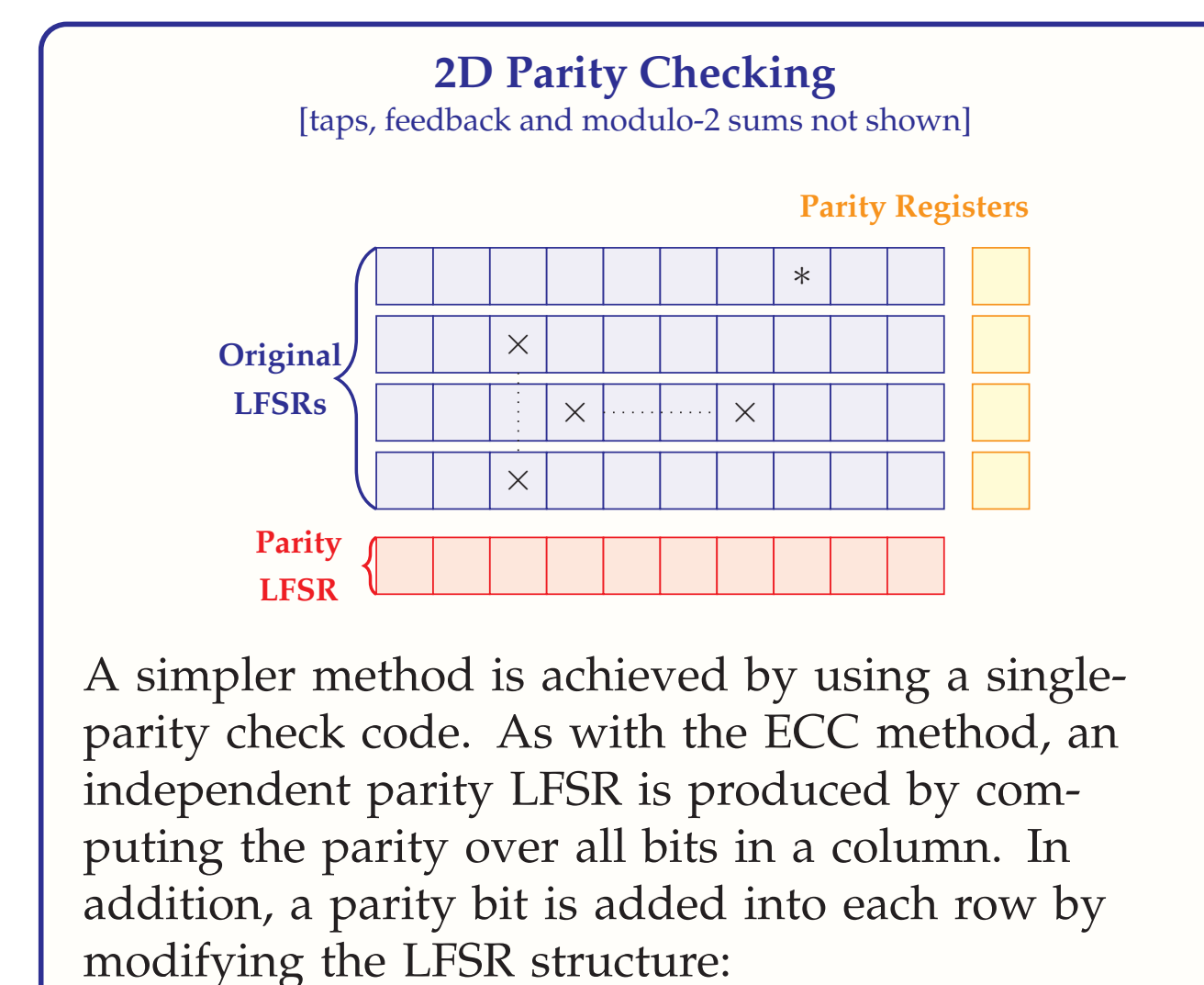
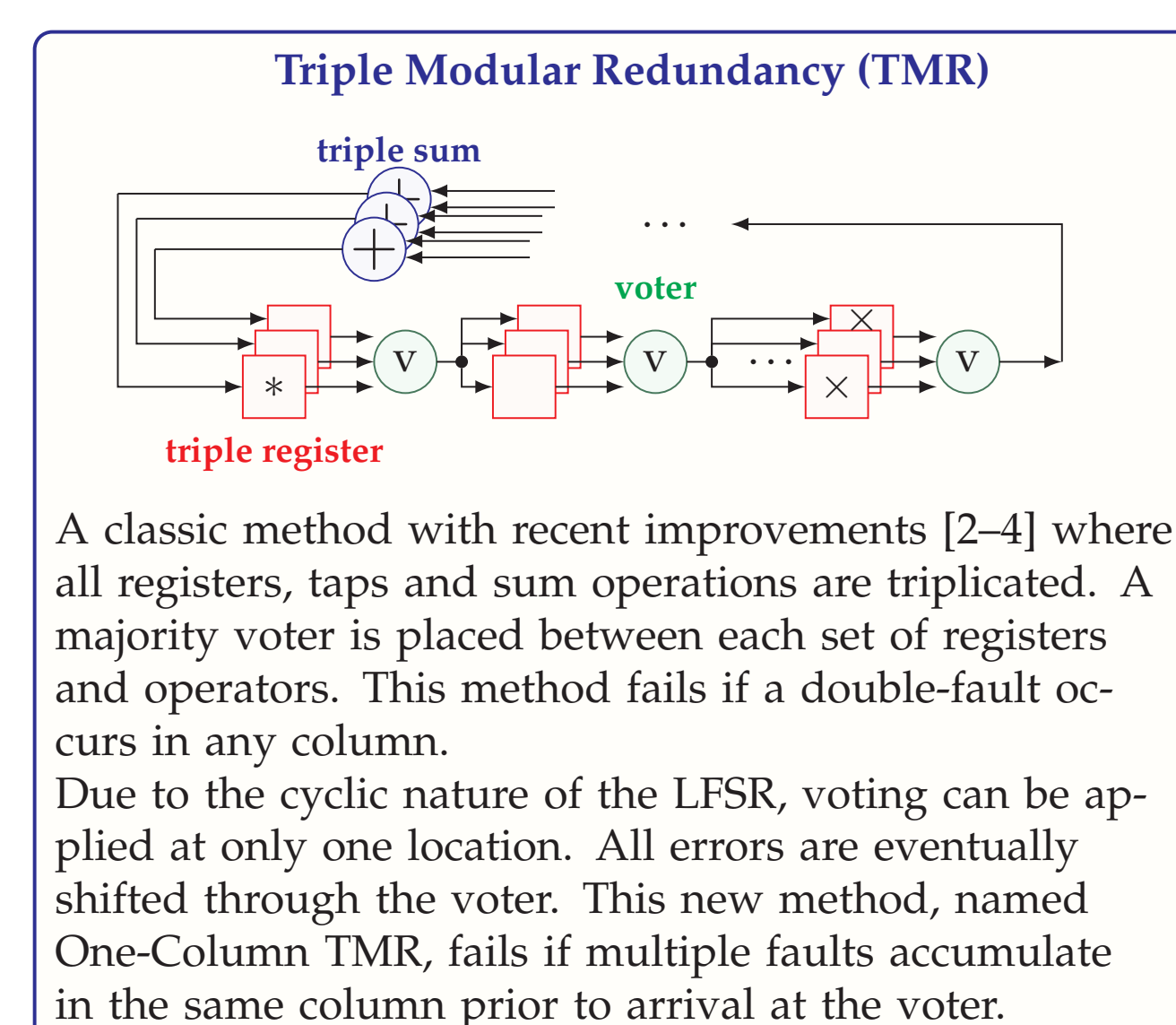


Top Level of the simplified tracking channel module; Error tolerance has been already studied in components with warning marks at the output. The corresponding proposed techniques are presented and evaluated in papers beside each mark.

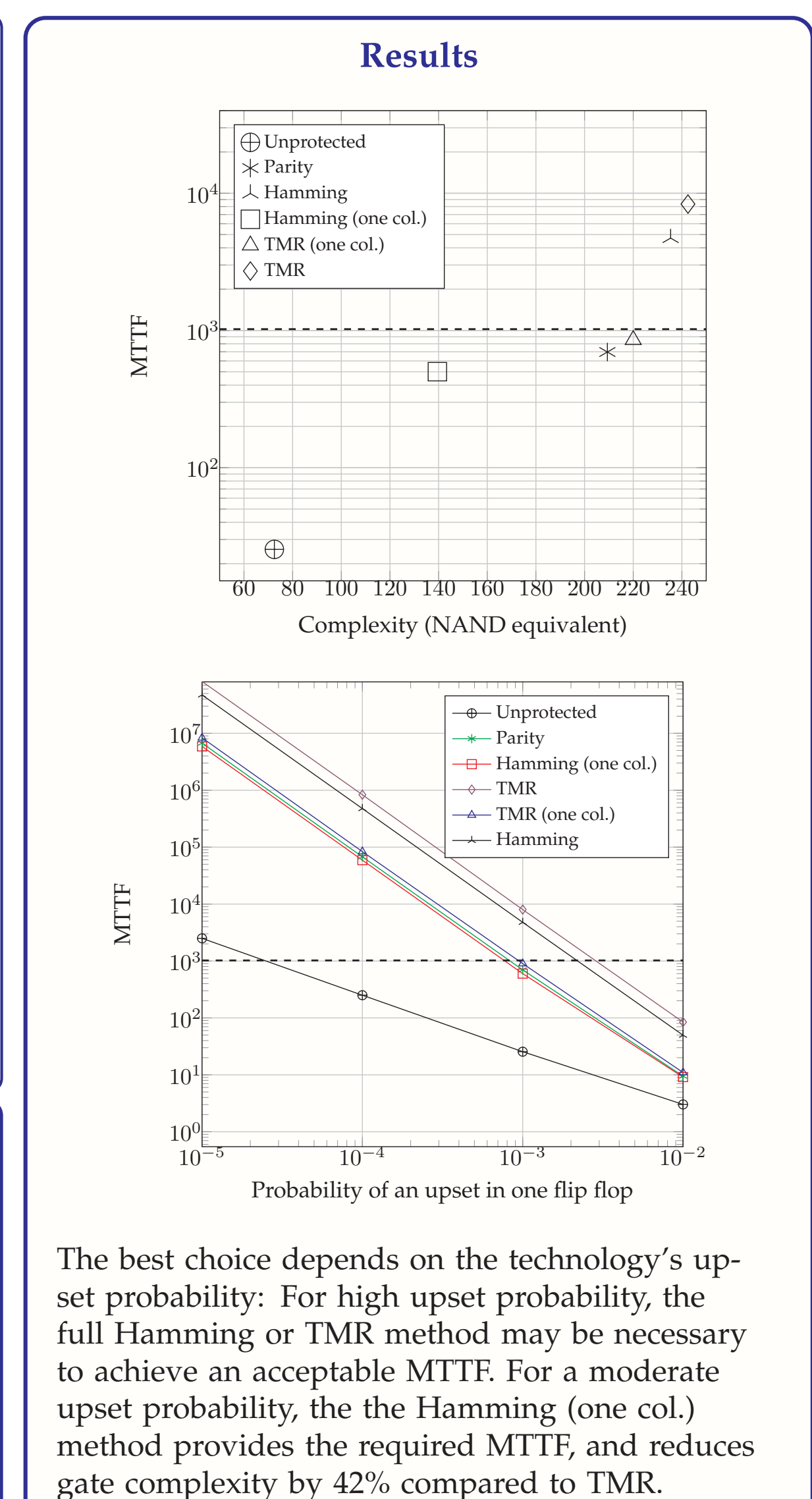


G1 sequence generator

## RELIABLE LFSRS



**Evaluation: Mean Time to Failure (MTTF)**  
Each method will fail under a variety of fault patterns. Since the GPS Gold sequences have a period of 1023, the LFSRs can be reset to a known state each period. Hence **reliable function is needed for at least 1023 clock cycles**. MTTF was solved for each method using the analytical techniques described in [6]. Logic synthesis was done to express complexity in terms of equivalent NAND gates for each case.



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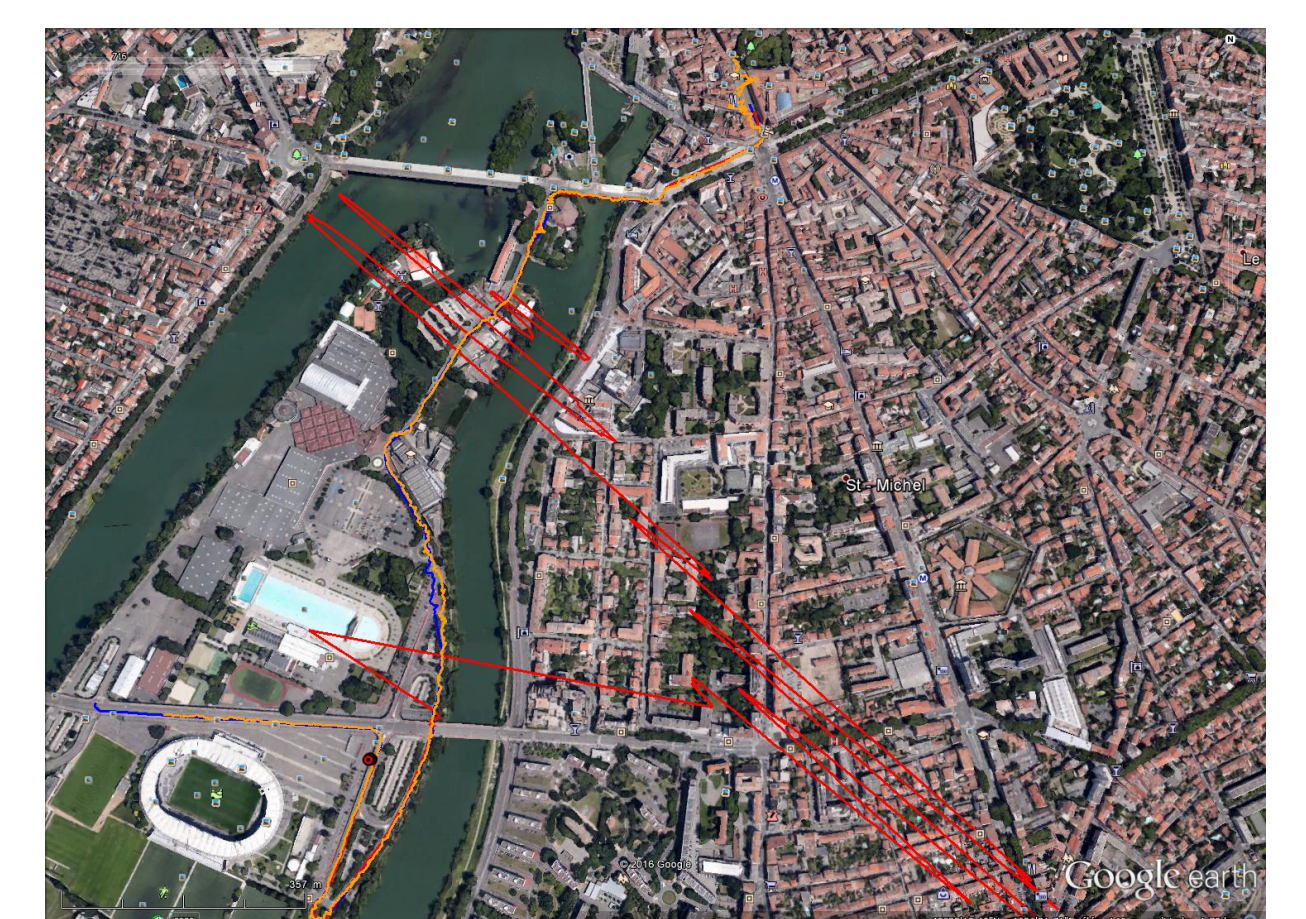
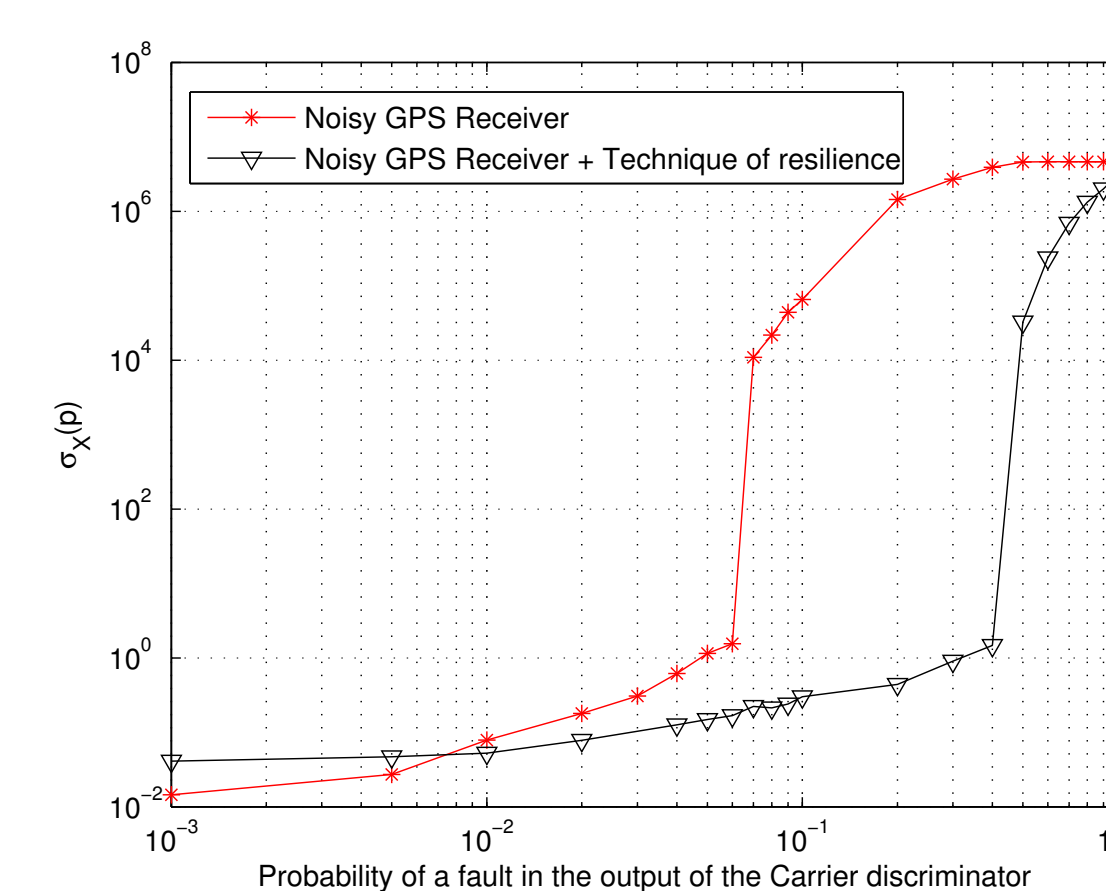
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## RELIABLE CARRIER DISCRIMINATOR

- Tuning the carrier filter bandwidth yields to an important improvement in the robustness of GPS tracking loops against faults in the carrier discriminator computation.
- With 40 % of upset errors, the error in the position between the noiseless and the noisy GPS receiver,  $\sigma_X(p)$ , does not exceed 2m while the reference GPS receiver does not support more than 6 % of errors [7].



## DESCRIPTION OF THE SIMULATION PLATFORM

The GPS receiver algorithm was first designed with the MATLAB high level software. Then, an implementation of the GPS receiver algorithm is done for an FPGA target to explore low level performances compared to the high level Matlab performances. The implemented platform can be split into three main parts:

- **User interface:** This represents the space from where the FPGA is controlled. The interface is written by MATLAB software. Functionality given by the user interface are: Program the FPGA with new codes, launch simulations, plot results, display position of a GPS receiver over time using Google Earth software...
- **Signal source file:** Signal received from more than 4 GPS satellites, over a significant period of time, are stored in a file. This file is added then in the memory of an FPGA to replace a real-time receiving process of a GPS receiver.
- **FPGA target:** this part will contain the hardware description of the acquisition and the tracking algorithms for a GPS receiver. It contains also a micro-blaze that manage the communication between the user interface and the hardware description of the GPS receiver.

